Google Scholar BETA

Web Images Video News Maps more »

pipelined "virtual router" - 2002 Search

Search only in Engineering, Computer Science, and Mathematics.
Search in all subject areas.

Scholar All articles - Recent articles Results 1 - 29 of 29 for pipelined "virtual rou

Pipe lined static router and scheduler for configurable logic system performing simultaneous ...
CW Selvidge, A Agarwal, J Babb, ML Dahl - US Patent 5,850,537, 1998 - freepatentsonline.com
... A row corresponds to a pin and each column to a pipeline clock period ... use count represents the number of channel path conductors used by the virtual router at a ...
Cited by 24 - Related articles - Web Search - All 6 versions

Building a robust software-based router using network processors - ▶ atl.ga.us [PDF]
T Spalink, S Karlin, L Peterson, Y Gottlieb - Proceedings of the eighteenth ACM symposium on Operating ..., 2001 - portal.acm.org
... 3.1 Forwarding Pipeline The common unit of data transferred through the IXP1200 is a 64-byte MAC-Packet (MP). ... Figure 4 summarizes the forwarding pipeline. ...
Cited by 159 - Related articles - Web Search - BL Direct - All 30 versions

Virtual processor techniques in a SIMD multiprocessor array
GL Steele Jr, WD Hillis, G Bleiloch, M Drumbeller, ... - 1989 - freepatentsonline.com
... 4,773,038; and "Pipelining Technique and Pipelined Processes for Multi-Dimensional Processor ... of the message format supplied to the virtual router in accordance ...
Cited by 26 - Related articles - Web Search - All 3 versions

Applying parallel discrete event simulation to network emulation
R Simmonds, R Bradford, B Unger - Parallel and Distributed Simulation, 2000. PADS 2000. ..., 2000 - ieeexplore.ieee.org
... as, for example, one or more simulated IP packets passes along the pipeline. ... to resolve the (ficticious) IP address and send packets to the virtual router. ...
Cited by 49 - Related articles - Web Search - All 6 versions

NetBind: a binding tool for constructing data paths in network processor-based routers - ▶ sinica.edu.tw [PDF]
AT Campbell, ST Chou, ME Kounavis, VD Stachtos, J ... - Open Architectures and Network Programming Proceedings, 2002 ..., 2002 - ieeexplore.ieee.org
... A network processor specification augments the virtual router specification with information about the ... A processing pipeline is a set of components that are ...
Cited by 50 - Related articles - Web Search - All 10 versions

A fast, simple router for the Data-Intensive Architecture (DIVA) system - ▶ hmc.edu [PDF]
CW Kang, J Draper - Circuits and Systems, 2000. Proceedings of the 43rd IEEE ..., 2000 - ieeexplore.ieee.org
... Each virtual router contains controlling logic, consisting of an input controller,

switch, and output con ... 5] Mike Galles, "Scalable Pipelined Interconnect for ...
Cited by 6 - Related articles - Web Search - BL Direct - All 5 versions

Performance Evaluation of VCRI. Sc: a Virtual Router for Transputer Networks

JP KTTAJ1MA, B PLATEAU - Transputers'92: Advanced Research and Industrial ..., 1992 - books.google.com
... Sc: a Virtual Router for Transputer Networks Joao Paulo KTTAJ1MA" Brigine PLATEAU Laboratoire de Ginie ... by VCR (the physical links are used in a pipelined mode ...
Related articles - Web Search

System and method for hierarchical metering in a virtual router based network switch

Z Hussain, S Desai, N Alam, J Cheng, T Millet - US Patent App. 10/163,162, 2002 - Google Patents
... 5/6 SEND PACKET TO NEXT PIPELINE STAGE s Page 7. US 2003/0223361 Al Dec. 4, 2003
SYSTEM AND METHOD FOR HIERARCHICAL METERING IN A VIRTUAL ROUTER BASED NETWORK ...
Related articles - Web Search - All 4 versions

Method and apparatus for multi-redundant router protocol support

TS Michels, D Clear, J Cathey - EP Patent 1,158,725, 2001 - freepatentsonline.com
... virtual router groups and more than four VRRP virtual router groups simultaneously ... the application engine 206 preferably has a pipelined architecture wherein ...
Related articles - Web Search - All 3 versions

Method and apparatus for multi-protocol redundant router protocol support

D Clear, T Michels, J Cathey - US Patent App. 09/815,603, 2001 - Google Patents
... HSRP virtual router groups and more than four VRRP virtual router groups simultaneously
on ... the application engine 206 preferably has a pipelined architec- ture ...
Web Search

A case study of Web server benchmarking using parallel WAN emulation - ucalgary.ca [PDF]

C Williamson, R Simmonds, M Arlitt - Performance Evaluation, 2002 - Elsevier
... the interface in promiscuous mode is that a virtual router address and ... connection, either serially (persistent connection) or in a pipelined fashion (pipelined ...
Cited by 16 - Related articles - Web Search - All 10 versions

[PDF] Building a parallel computer system for $18,000 that performs a half peta-flop per day

FH Bennett III, JR Koza, J Shipman, O Stiffelman - Proceedings of the Genetic and Evolutionary Computation ..., 1999 - genetic-programming.com
... The Parsytec virtual router creates a toroidal mesh among the 64 processing nodes. ... The instruction units are pipelined and able to produce a result on every ...
Cited by 48 - Related articles - View as HTML - Web Search - All 7 versions

APAP I/O programmable router

CA Collins, MC Dapp, JW Dieffenderfer, DC ... - US Patent 5,963,745, 1999 - freepatentsonline.com
... method thereof. 4984237, January, 1991, Franaszek, 370/388, Multistage network

with distributed pipelined control. 4985832, January, 1991, ...
Cited by 10 - Related articles - Web Search - All 5 versions

Content service aggregation system control architecture
E Ganesan, R Penwar, Y Lee, C Am Nguyen, J ... - US Patent App. 10/191,746, 2002 - Google Patents
Page 1. US 20030069973A1 (19) United States (12) Patent Application Publication (io> Pub. NO.: US 2003/0069973 Al Ganesan et al. (43) Pub. Date: Apr. ...
Web Search

Technology challenges for virtual overlay networks - ▶mtu.edu [PDF]
KP Birman - Systems, Man and Cybernetics, Part A, IEEE Transactions on, 2001 - ieeexplore.ieee.org
... solution would provide the necessary properties, but nothing in the pipeline offers an ... and treated as if it resides entirely within a virtual router defined by ...
Cited by 5 - Related articles - Web Search - BL Direct - All 12 versions

The Next-Generation Internet: Unsafe at Any Speed? - ▶cornell.edu [PDF]
KP Birman - COMPUTER, 2000 - doi.ieeecs.org
... But nothing in the pipeline offers an easy answer for other noninterference goals ... and treated as if it resides entirely within a virtual router defined by the ...
Cited by 14 - Related articles - Web Search - BL Direct - All 8 versions

Multi-Transputer Systems with Dynamic Link Connection Switching Controlled through a Serial Bus
MTT Kalinowski - Transputer Applications and Systems' 93: Proceedings of the ..., 1993 - books.google.com
... of transputer links for reconfiguration control than in the pipeline-based system ... Plateau, Performance Evaluation of VCR 1.8 c: a Virtual Router for Transputer ...
Related articles - Web Search

Advanced parallel array processor (APAP)
TN Barker, CA Collins, MC Dapp, JW Dieffenderfer, ... - US Patent 5,717,943, 1998 - freepatentsonline.com
... and wherein an array of nodes is provided with means for directed inter-processor memory element communication for preparing data for pipelined very high speed ...
Cited by 40 - Related articles - Web Search - All 7 versions

[PDF] ▶An IP-Multicast based Framework for Designing Synchronous Distributed Multi-User Applications on the ...
P Parnes - 1999 - sm.luth.se
Page 1. An IP-Multicast based Framework for Designing Synchronous Distributed Multi-User Applications on the Internet Peter Parnes NOVEMBER 1999 ...
Cited by 4 - Related articles - View as HTML - Web Search - Library Search - All 10 versions

Fully distributed processing memory element
TN Barker, CA Collins, MC Dapp, JW Dieffenderfer, ... - US Patent 5,963,746, 1999 - freepatentsonline.com
... and wherein an array of nodes is provided with means for directed inter-processor memory element communication for preparing data for pipelined very high speed ...
Cited by 15 - Related articles - Web Search - All 3 versions

SIMD/MIMD processing memory element (PME)
TN Barker, CA Collins, MC Dapp, JW Dieffenderfer, ... - US Patent 5,625,836, 1997 - freepatentsonline.com
... 4916652, April, 1990, Schwarz, 364/748, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream ...
Cited by 18 - Related articles - Web Search - All 3 versions

SIMD/MIMD array processor with vector processing
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,966,528, 1999 - freepatentsonline.com
... 4916652, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream single data architectures, ...
Cited by 12 - Related articles - Web Search - All 3 versions

Parallel processing system having asynchronous SIMD processing and data parallel coding
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,761,523, 1998 - freepatentsonline.com
... 4916652, April, 1990, Schwarz, 364/748, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream ...
Cited by 7 - Related articles - Web Search - All 3 versions

Fully scalable parallel processing system having asynchronous SIMD processing
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,752,067, 1998 - freepatentsonline.com
... 4916652, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream single data architectures, ...
Cited by 7 - Related articles - Web Search - All 3 versions

Autonomous SIMD/MIMD processor memory elements
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,717,944, 1998 - freepatentsonline.com
... 4916652, April, 1990, Schwartz, 364/748, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream ...
Cited by 7 - Related articles - Web Search - All 3 versions

SIMD/MIMD inter-processor communication
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,708,836, 1998 - freepatentsonline.com
... 4916652, April, 1990, Schwarz, 364/748, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream ...
Cited by 10 - Related articles - Web Search - All 3 versions

Parallel processing system having asynchronous SIMD processing
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,754,871, 1998 - freepatentsonline.com
... 4916652, April, 1990, Schwarz, 364/748, Dynamic multiple instruction stream multiple data multiple pipeline apparatus for floating-point single instruction stream ...
Cited by 8 - Related articles - Web Search - All 3 versions

Parallel processing system having a synchronous SIMD processing with processing elements emulating ...

PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,765,011, 1998 - freepatentsonline.com
A parallel array processor for massively parallel applications is formed with low power CMOS with DRAM processing while incorporating processing elements on a single ...
Cited by 8 - Related articles - Web Search - All 3 versions

Array processor with asynchronous availability of a next SIMD instruction
PA Wilkinson, JW Dieffenderfer, PM Kogge, NJ ... - US Patent 5,870,619, 1999 - freepatentsonline.com
A parallel array processor for massively parallel applications is formed with low power CMOS with DRAM processing while incorporating processing elements on a single ...
Cited by 8 - Related articles - Web Search - All 3 versions

Key authors: T Spalink - S Karlin - L Peterson - Y Gottlieb - R Simmonds

pipelined "virtual router" Search

Google Home - About Google - About Google Scholar